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PRINTER RUSH

(PTO ASSISTANCE)

Application : 10/04/013 Examiner : Chen, Tse GAU : 2116
From : 6/26 Location : IDC FMF FDC Date : 4/20/05
Tracking # : 06092672 Week Date : 4/14/05

DOC CODE	DOC DATE	MISCELLANEOUS
<input type="checkbox"/> 1449		<input type="checkbox"/> Continuing Data
<input type="checkbox"/> IDS		<input type="checkbox"/> Foreign Priority
<input checked="" type="checkbox"/> CLM	<u>12/20/2004</u>	<input type="checkbox"/> Document Legibility
<input type="checkbox"/> IIFW		<input type="checkbox"/> Fees
<input type="checkbox"/> SRFW		<input type="checkbox"/> Other
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[RUSH] MESSAGE: ① Claim 6 (original) does not end with a period
② Please provide the serial number to fill in the blank spaces
on page 14, line 17 of specification

[XRUSH] RESPONSE: CA

INITIALS: MA

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REV 10/04

4/21/05
5/1/05

MULTIPLE MODE POWER THROTTLE MECHANISM

Related Patent Applications

This patent application is related to U.S. Patent Application No. 10/041,292, "Digital

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5 Throttle for Multiple Operating Points", filed on even date herewith and assigned to the same assignee.

Background of the Invention

Technical Field The present invention relates to microprocessors and, in particular, to mechanisms for controlling power consumption in microprocessors.

Background Art. Modern processors include extensive execution resources to support concurrent processing of multiple instructions. A processor typically includes one or more integer, floating point, branch, and memory execution units to implement integer, floating point, branch, and load/store instructions, respectively. Register files and on-chip caches are also provided to supply the execution resources with operands. When fully engaged by an executing program, these resources can create significant power dissipation problems.

Instruction code sequences that include enough instructions of the correct type to fully engage a processor's execution resources for significant intervals are relatively rare. Smart compilers and out of order execution can only extract so much instruction level parallelism (ILP) from most code. To conserve power, a processor may employ a clock gating mechanism to cut
20 off the clock signal delivered to execution resources or their components that are not used by an executing code sequence. Such a processor can engage extensive resources as needed, e.g., to support code sequences with high ILP, without dissipating large amounts of power when code sequences with more typical ILP levels execute.

efficacy of a power control mode that is currently operative, and mode selector 550 selects which, if any, power control mode is operative, based on inputs from TU 250 and SU 510.

The disclosed embodiment of SU 510 includes an adder 514, a reset unit 518, an accumulator 520, and comparators 530(a), 530(b) and threshold stores 534(a), 534(b). Adder 514 and reset unit 518 monitor the output of TU 350 to determine whether or not the first power control mode is engaged. Accumulator 520 increments or decrements a stored value, according to whether or not the first power control mode is engaged. The stored value indicates how often the first power control mechanism is being engaged. If this value reaches a first threshold, e.g. the value in store 534(a), the first control mode is being activated too frequently, and a second control mode is warranted. If this value reaches a second threshold, e.g. the value in store 534(b), the second control mode is no longer necessary. First and second comparators 530(a) and 530(b) assert their signals to mode selector 550, which adjusts the control modes accordingly.

For one embodiment of the digital throttle the first control mode adjusts instruction throughput (ITP) and the second control mode adjusts the processor's operating point (OP). One mechanism for adjusting instruction throughput is to inject no-operations (NOPs) into the execution pipeline of the processor. U.S. Patent Application No. 10/41092 describes one mechanism for injecting NOPs.

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For a multi-mode digital throttle that employs instruction throughput rates and operating points to control power consumption, mode selector 550 may implement the actions summarized in Table 1. Here, AL refers to the (scaled) activity level tracked by AM 330 and TC refers to the throttle count tracked by mode unit 380.